Amendments to the Specification:

Page 1, line 1, delete the paragraph consisting solely of the word "Specification".

Page 1, add the following as the first sentence of the specification:

--RELATED APPLICATIONS:

This is a U.S. national stage of International application No. PCT/DE00/00276 filed 01 February 2000.

This patent application claims priority of German Patent Application No. 19908414.9 filed 26 February 1999, the disclosure of which is hereby incorporated by reference.--

Page 1, lines 3-5, delete the paragraph beginning with "The invention relates to" and replace it as follows:

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to an optimized bus connection for acceptance of bus transactions.

(2) Description of Related Art

Page 1, line 28 to page 2, line 2, replace the paragraph beginning with "The object of the present invention" as follows:

SUMMARY OF THE INVENTION

[[The]] One object of the present invention is to provide an optimized bus connection, by which the working speed of a processor system is accelerated and thus its performance capability is increased.

Page 2, lines 3-5, delete the paragraph beginning with "Starting from a bus connection" and replace it as follows:

This and other objects are attained in accordance with one aspect of the invention directed to an optimized bus connection for acceptance of bus transactions, provided with a first store operating according to a FIFO principle, in which bus transactions arriving from a higher-level processor system for execution by the optimized bus connection are temporarily stored in their sequence of arrival. A first functional section is coupled to an output of the first store for classifying the bus transactions temporarily stored in the first store, and including means for classifying those transactions that must be executed in a strictly logical sequence as a first class of transactions, and those transactions that do not have to be executed in a strictly logical sequence as a second class of transactions. A second functional section is coupled to an output of the first functional section and comprises at least first and second functional lines disposed in parallel, wherein the first functional line is allocated to the first class of transactions, and is provided with a storage structure functioning according to the FIFO principle, and wherein the second functional line is allocated to the second class of transactions, and has a storage structure suitable for random accesses. A third functional section, with an execution unit, is coupled to the functional lines of the second functional section, and comprising means for organizing the transactions allocated to the at least first and second function lines of the second functional section into a serial sequence for forwarding to the higher-level processor system, wherein the organizing means of the execution unit moves a transaction of

the second class ahead of a transaction of the first class, depending on a state of the higher-level processor system.

Page 2, lines 21-22, delete the paragraph beginning with "Advantageous embodiments".

Page 3, lines 12-15, delete the paragraph beginning with "A practical example of the invention" and replace it as follows:

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is schematic block diagram showing one embodiment of an optimized bus connection constructed in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWING

Page 3, lines 19-22, replace the paragraph beginning with "To processor bus PB" as follows:

To processor bus PB there is connected a first ~~temporary~~ store S1, which is known in itself and operates as a temporary store according to the FIFO principle, and which stores the arriving bus transactions in their sequence of arrival.

Page 4, lines 8-12, replace the paragraph beginning with "Second functional section" as follows:

Second functional section II receives, according to typification and classification, in one of three further stores including second store S2, third store S3, and fourth store S4, each of which is disposed in its own allocated functional line, the transaction processes typified and classified by decoder DK.

Page 4, lines 13-18, replace the paragraph beginning with "The transactions classified" as follows:

The transactions classified in the "execution in strictly logical sequence" class are received in second store S2 regardless of whether they correspond to the "write" or "read" type. Since these transaction processes must be executed in strictly logical sequence, a deeper-level subdivision into such types is not useful.

Page 5, lines 4-15, replace the paragraph beginning with "In the present practical example" as follows:

In the present practical example, transaction processes of the "execution not in strictly logical sequence" class and of the "read" type are stored in third store S3 of second functional section II. Since the sequence of execution is unrestricted, third store S3 is designed according to a parallel structure, from which contents can be extracted optionally. The same is true for fourth store S4 of second functional section II, only in regard to the "write" type with the "execution not in strictly logical sequence" transaction class. Since fourth store S4 is responsible for transaction processes of the "write" type, a second write store SS2 is allocated to this store in a manner corresponding to first write store SS1.

Page 5, lines 16-21, replace the paragraph beginning with "Stores S3 and S4" as follows:

Third store ~~Stores~~ S3 and fourth store S4 ensure that, in particular, the transactions of the "execution not in strictly logical sequence" class and of the "read" type can be executed immediately

and the transaction processes of the "execution not in strictly logical sequence" class of the "write" type can be executed as soon as possible.

Page 6, lines 6-16, replace the paragraph beginning with "Shortcuts KW1 and KW2" as follows:

Shortcuts KW1 and KW2 permit the transaction processes to jump over individual functional sections. For example, if the successive components of functional sections I and II are empty, a transaction process can travel directly from processor bus PB via shortcut KW1 into execution unit AE of functional section III. If second store S2 operating according to the FIFO principle in functional section II is empty, an arriving transaction process can be transferred immediately through the store and directed to execution unit AE of functional section III. In both cases, time is saved for transaction processes which affect through transport.